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Design of Shift Register with Minimized Area by Using 4 Bit Hybrid Latch

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Abstract: - SHIFT REGISTERS has been used as a gateway for designing very high-speed VLSI circuits. It is designed using the efficient pulsed latch technique. Efficient pulsed latch is replacement of flip-flops with hybrid latch. It has single phase clock and triggering on one edge. This paper proposes hybrid latch flip flop design to redu ce power consumption with use of smaller flip flops thus the area will be minimized. Shift register has been designed in 16nm CMOS technology.

Key Words — *Phase clock, flip flop, latch.*

I. INTRODUCTION

SHIFT Registers are widely used in VLSI circuits and it has been used in application such as digital filters, communication receivers and image processing, where shift registers are the simple architecture that reduces the area and power of the circuits.

Architecture of shift register is composed of a series connected flip-flops. Because it shares the same clock. The output of each flip flop is connected to the input of the next flip flop. Thus, it saves the data and the timing problem.

This paper proposes the shift register design using the hybrid latch flip flop instead of pulsed latch technique. By using the hybrid latch area is minimized.

This paper is organized as follows, section II introduces the shift register using pulsed latch, section III Design of Hybrid latch. In section IV discuss the simulation and layout of hybrid latch and section V concludes the paper.

II. PULSED LATCH

Pulsed latches share the pulse generated circuit for the pulsed clock signal thus the power consumption of the circuit will be minimized along with occupied area.

It has been replaced in the circuit instead of flip flop in many applications, because it is much smaller than flip flops.

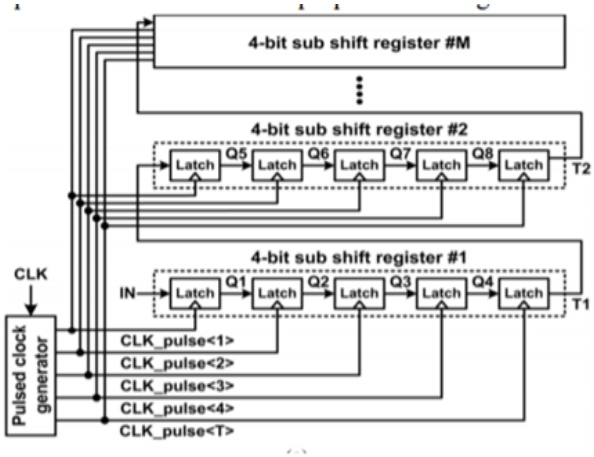

Fig.1.Architecture of Shift Register Using Pulsed Latch

III. HYBRID LATCH

Hybrid latch Flip Flop is the best pulse triggered flip flops. It reduces the timing problem of the pulsed latch design.

Pulsed latch does not be connected to the shift register because of the timing problem. Only the non-overlapped delay unit will overcome this issue.

To design four-bit shift register the 4-bit hybrid latch were used it has the single-phase clock and the data dependency and transparency is high.

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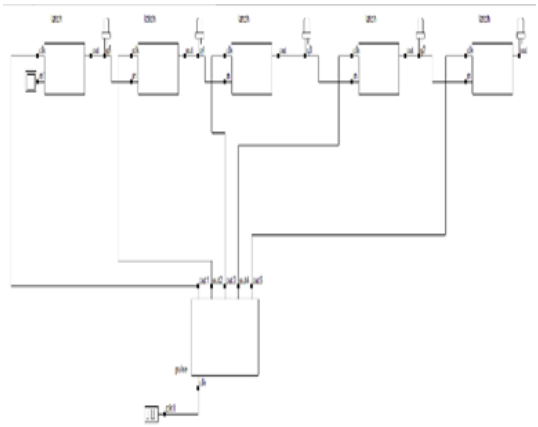

Fig. 2. Basic Structure of Hybrid Latch

IV. Simulation And Layout Of Shift Register

A. Layout of Shift Register with Pulsed Latch-Switches

Before implementing the circuit, schematic is generated in DSCH3. It is a logic editor and simulator used of architecture of logic design.

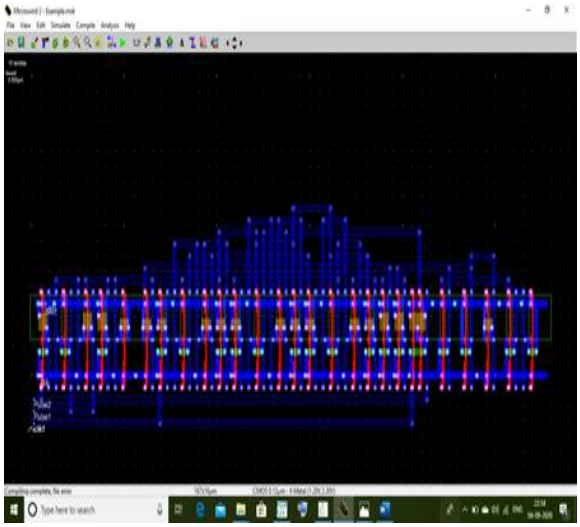

Fig.3. Schematic layout of pulsed latch shift register

B. Simulation Result of Pulsed Latch-Switches

Simulation analysis in micro wind 2 is compiled and waveform was analyzed with 120 nm CMOS technology and the power consumption is about 0.110MW.

Fig.4. Simulation output of pulsed latch-Sw

C. Layout of Shift Register with Pulsed Latch-MUX

Layout of pulsed latch with using of mux is seen by the microwind 2 it is also in the 120 nm CMOS technology with power consumption of 0.110mW.

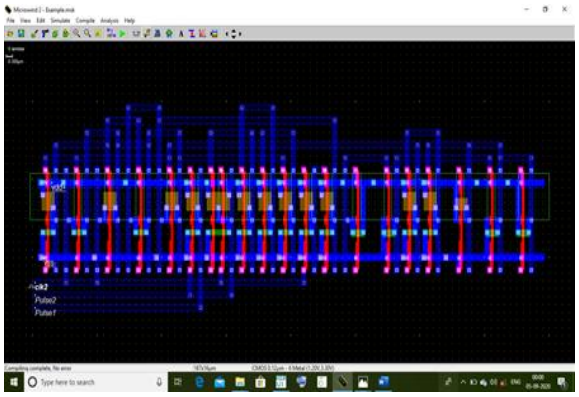

Fig.5. Schematic layout of pulsed latch using mux

D. Simulation Result of Pulsed Latch- MUX

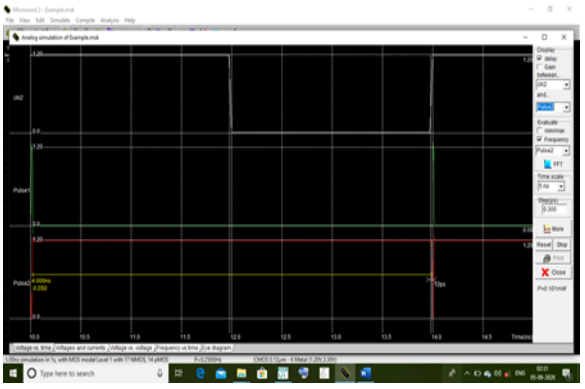

Fig.6. Simulation output of pulsed latch mux

E. Layout of Hybrid Latch

Schematic view of hybrid latch has been seen using the Microwind 2 with 16 nm CMOS technology.

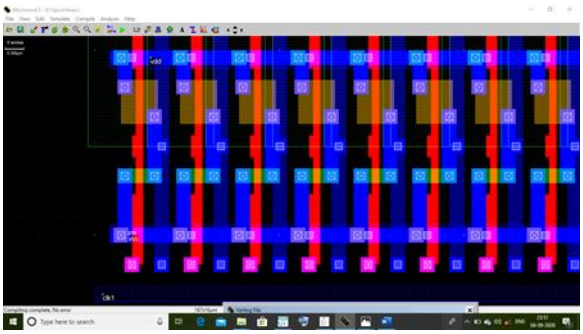

Fig .7. Schematic layout of Hybrid latch

F. Simulation Result of Hybrid Latch

The simulation result of shift register was Latch implemented using the 4-bit hybrid latch. In this method the area is minimized about 16nm and the power consumption is 0.158Mw.

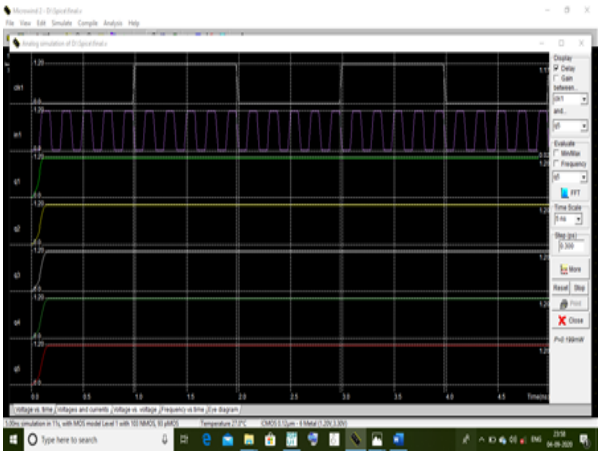

Fig.8. Simulation output of hybrid latch

V. CONCLUSION

This paper concludes that shift register is designed using the Hybrid latch. In this the number of flip flops are very less so that area will be minimized at the same time due the single phase clock usage timing error is minimized.

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