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Low –Power Low–Voltage Asynchronous Delta–Sigma Modulator

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Abstract: - Due to the increase in the ultralow - power VLSI systems this work is one of the solution for the ultralow - voltage bulk driven (BD) asynchronous delta – sigma modulator which is implemented in 54nm CMOS technology with V_{DD} supply as 300 mV, the circuit leads to the total power consumption of 15.35 pW. The above mentioned result have been achieved employing a highly linear transconductor (Gm – C) as an integrator it is as similar as an R – C integrator, asynchronous delta – sigma modulator (ADSM) and a hysteretic comparator based on non - tailed BD differential pair with un buffered op-amps since it has very high output resistance than buffered op-amp. The main objective of this paper is to offer good accuracy even at low supply voltages with good frequency response.

Key Words — ***Bulk driven asynchronous delta-sigma modulator, Linear transconductance integrator, Hysteric Comparator, Buffered op-amps, Unbuffered op-amps, Ultralow-power VLSI systems.***

I. INTRODUCTION

With the significant increase in the ultralow – power and ultralow – voltage VLSI systems, the supply voltages are made as low as 0.25 – 0.3 volts. In order to meet the requirements posed by such sources, a number of innovative circuit solutions have recently been developed, one of such sources is reviewed in this paper. In order to meet the requirements, the solutions mostly including unbuffered op-amps, linear transconductors and delta – sigma modulators (DSMs) are used with the concept of bulk driven transistors. The most interesting solutions include unbuffered op-amps [1], [2], linear transconductors [3], [4], and delta–sigma modulators (DSMs) [5]– [7]. Among different architectures, the asynchronous delta – sigma modulators (ADSM) have gained most advantages in recent years. One of the greatest challenges for analog designers dealing with sub-0.5-V circuits is the realization of power efficient and precise analog-to-digital converters (ADCs). ADSMs translates band-limited analog input signal to an asynchronous modulated square wave which doesn't require clocking and offers good accuracy at even low supply voltages. Owing to its principle of operation, the circuit has a simple structure, does not require any clocking, is free of quantization noise, has good frequency response, and offers good accuracy at very low supply voltages [8]–[10]. It is also worth to point out that ADSM architecture is well sufficiently compatible with contemporary CMOS technologies. An interesting approach to the design of an ULV ADSM based on BD building blocks and exploiting a single-ended RC integrator has recently been proposed in [6]. The circuit offers reasonable performance in an ULV environment, nevertheless, it was realized using low VTH CMOS process and required several off-chip passive elements. The proposed circuit offers similar performance as the one described in [6] but can operate with much lower relative supply voltage (VDD/VTH). The fully differential architecture of this circuit allows reducing the even harmonics of the output signal, thus improving the linearity and consequently the resolution of ADSM. In addition, since the RC integrator in [6] has been replaced with a Gm–C integrator in the proposed design, the above-mentioned external RC elements applied in [6] are avoided, which is another advantage of the proposed solution. The design experimentally confirms proper operation of the transconductor [4] and the common-mode feedback (CMFB) circuit [12], which in original papers was validated only by simulations. In addition, a new ULV BD comparator has been designed and investigated. All the blocks were designed and optimized for application in ULV ADSM and the design tradeoffs for such application have been discussed. The design experimentally confirms the feasibility of the proposed circuits and investigates their performance in ULV ADSM.

II. ASYNCHRONOUS DELTA-SIGMA MODULATOR

Below is the block diagram of 1st order ADSM consists of linear trans-conductance integrator, DAC and comparator. The ADSM generates a square-wave output signal with both, the duty cycle 'd', and the oscillation period 'To' being functions of the input amplitude, according to the following formulas [8]:

$$d = \frac{1+u}{2} \quad (1)$$

$$T_0 = \frac{1}{f_0(1-u^2)} \quad (2)$$

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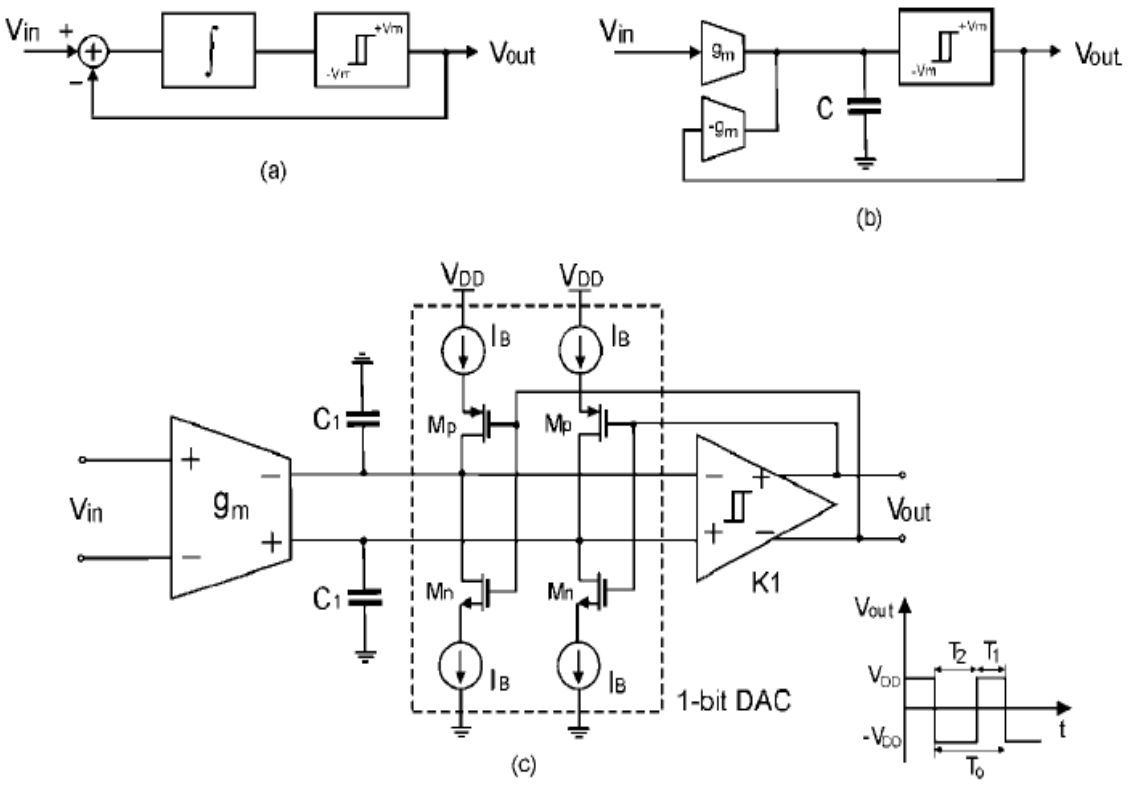

Fig. 1. (a) First-order ADSM. (b) Realization with linear transconductors. (c) Proposed fully differential ADSM.

Where, u = Vin/Vm is the normalized input amplitude, with the normalization voltage Vm equal to the output voltage level, and fo is the constant center frequency. The block diagram of the proposed fully differential ADSM is shown in Fig. 1(c). The circuit consists of a continuous time Gm–C integrator, a hysteretic comparator (K1), and a 1-bit digital-to-analog converter (1-bit DAC) in the form of the switched current sources IB, with transistors Mp and Mn operating as switches. Note that in the proposed realization, the feedback signal depends on the value of IB rather than the output voltage level as in Fig. 1(a), which makes the proposed circuit less sensitive to power supply variations. The duty cycle for the considered circuit is given as

$$d = \frac{T_1}{T_1 + T_2} = \frac{1+u}{2} \qquad (3)$$

while the total time period of the output square wave to is given as

$$T_0 = T_1 + T_2$$

The normalized input signal *u* can also be expressed in terms of T_1 and T_2 as

$$u = \frac{T_1 - T_2}{T_1 + T_2}$$

Hence, the input signal could easily be recovered by the measurement of the periods T_1 and T_2. This could be done with a reconstruction digital circuit [8].

III. TRANSISTOR LEVEL REALIZATION

A. $G_m - C$ Integrator

In this design, this integrator approach has been used to design a voltage integrator. This integrator provides better power efficiency and larger input resistance than their RC counterparts and allow avoiding large resistors which are difficult to integrate. The Gm–C integrator employed in the considered design [Fig. 2(a)] consists of the BD linear trans-conductor proposed in [4] and the CMFB circuit in [6]. The Gm stage is characterized by excellent linearity of its transfer characteristic, even for VDD as low as 0.25 V to 0.3 V.

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For all the p – channel transistors, the common mode voltage 'V_{CM}' is made equal to zero. Parameters for the integrator are given as follows for the operation of the circuit in Table I. The supply voltage for the circuit is between 0.25 volts.

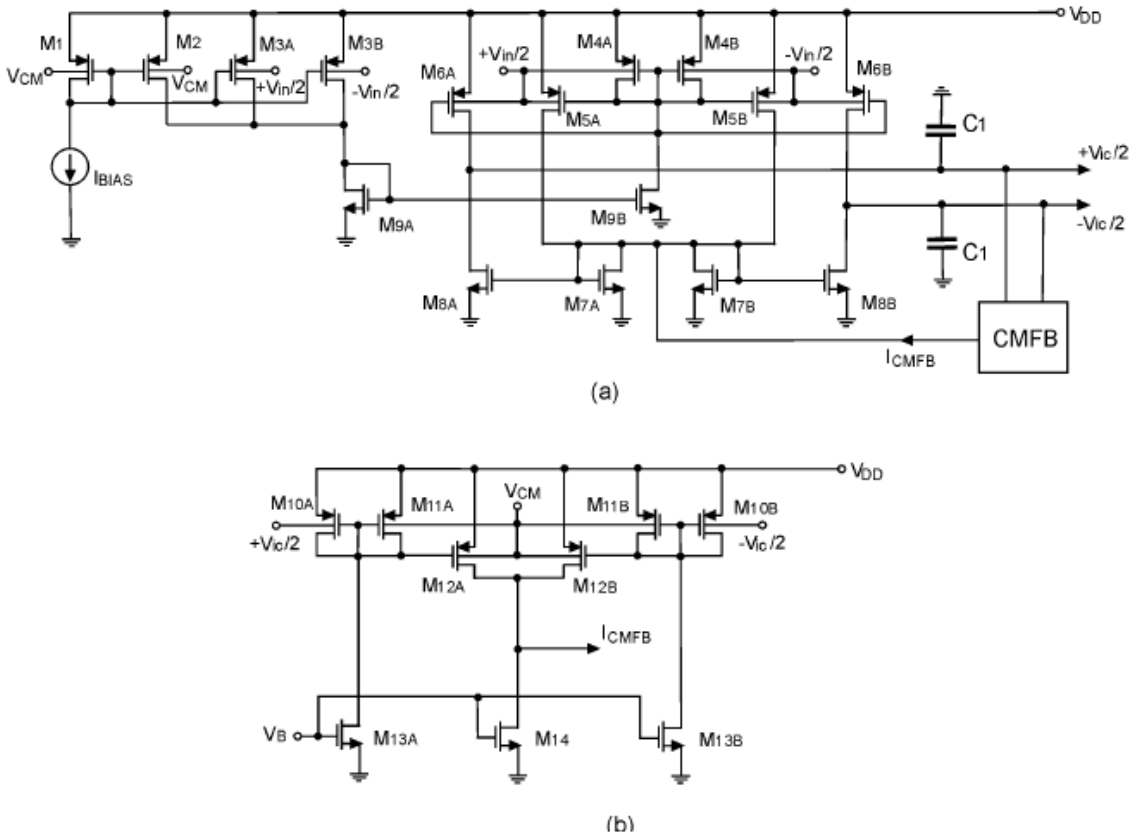

Fig. 2. (a) BD G_m–C integrator. (b) CMFB circuit.

Table.1. Parameters of Trans-Conductance Integrator

Parameter	Value
Bias Current	5 nA
Input Voltage	0.25 V
Common Mode Voltage	Made Zero
Drain Voltage	0.3 V
Power Consumption	15.2 pW

B. Hysteric Comparator

This comparator (Fig. 3) has been implemented using Bulk-Driven (BD) open loop amplifier connected with a negative resistance load (NRL). Input of the differential amplifier (M15 – M17) is supplied from digital to analog converter (DAC) with the support of Vic/2 from DAC circuit.

With the lack of current source at tail, which is a useful feature behaves as an absolute differential amplifier with high common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). With the addition of trans-conductance boosting circuitry ($M_{16\,A,\ B}$), DC voltage will get a gain of 6 dB when compared to common mode BD differential pair.

Built-in Hysteresis can be realized using the transistors M22–M23 using NRL circuit. The set of the current mirrors (M18–M22) is used to realize the differential output of the comparator. The additional inverters (Inv1 and Inv2) are used to further improve the quality of the output waveform. Fig. 4 shows the simulated dc transfer characteristic of the comparator, while Fig. 5 shows its transient response for different input voltages. As it can be

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noted, the time delay of the comparator () depends on the amplitude of the input signal and varies from 10 µs for Vin = 300 mV to 74 µs for Vin = 10 mV. Parameters of the comparator are summarized in Table II.

Table.2. Parameters of Comparator

Parameter	Value
Drain Voltage	0.3 V
Input Voltage	From DAC circuit
Power Consumption	155 nW

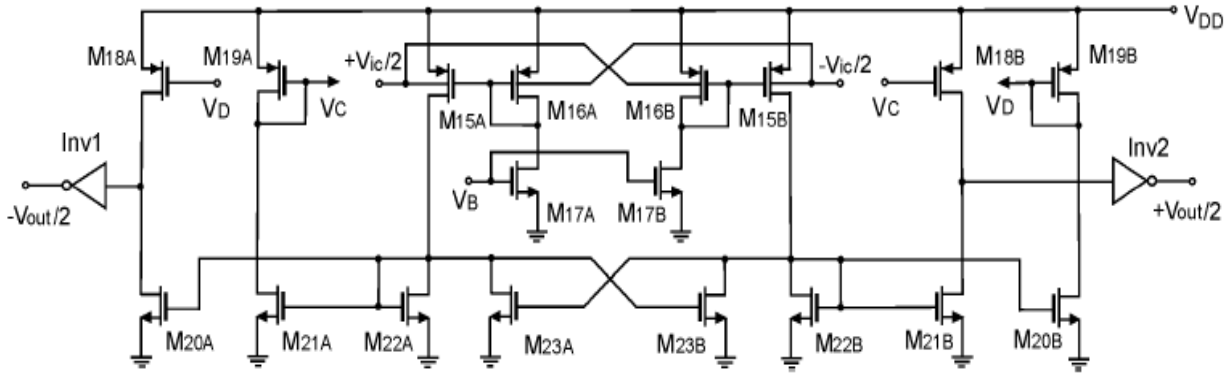

Fig. 3. BD hysteretic comparator.

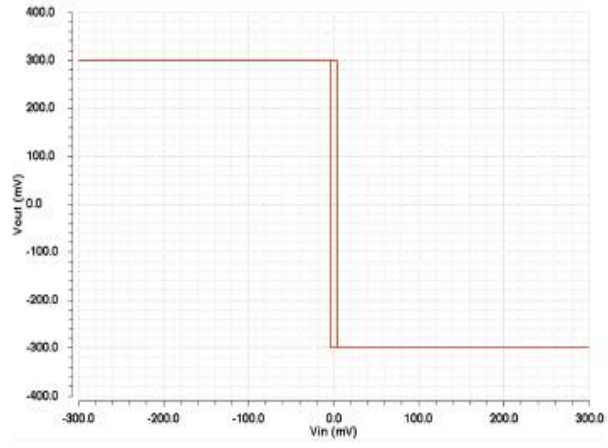

Fig. 4. Simulated dc transfer characteristic of the voltage comparator.

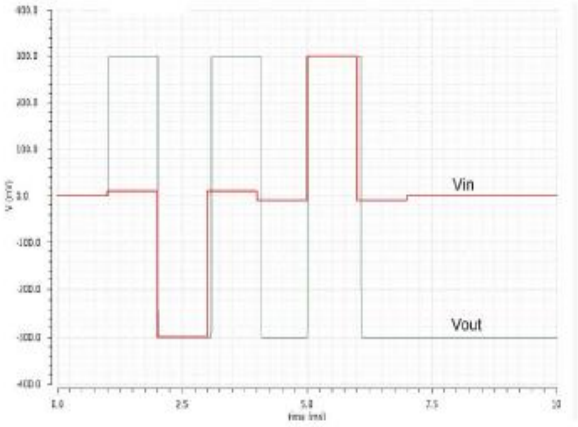

Fig. 5. Simulated time response of the voltage comparator.

C. 1 - bit DAC

The DAC circuit implemented in this work was shown in Fig. 6. This circuit was implemented using transistors consisting of four current sources / sinks $M_{24\,C,D}$, $M_{25\,B,C}$ and four switches $M_{26\,A,B}$, $M_{27\,A,B}$. The inputs to this circuit are given to switches which are controlled with the outputs of Asynchronous Delta – Sigma Modulator (ADSM).

Based on the output voltage levels, the DAC output current sink or source will be equal to I_b (5 nA). Therefore, the 1-bit DAC can be considered as a fully differential switched – current source. The mis-matched currents add up with each other thus increases the In_{out} offset of ADSM. This DAC circuit is mainly used for converting digital signals to analog signals in the form of bits. But, it converts only one bit per cycle. Therefore, if more the number of bits used in the circuitry; more the number of data will be generated with the

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help of very low power and very low voltage which is used highly in future use. The duty cycle of the generated results for Vin = 0 is given as follows.

$$\frac{T_1}{T_1+T_2} = \frac{1}{2}\left(1 + \frac{g_m V_{os}}{2I_B}\right)$$

Where, V_{os} is the inout offset of the ADSM.

The parameters of this 1-bit DAC are given in the below table-IV.

The complete parameters of all the transistors for the benefit of operation regarding the ratio of length and width are tabulated as follows.

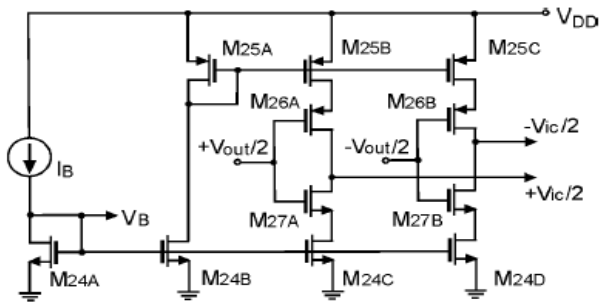

Fig. 6. 1-bit DAC circuit.

IV. EXPERIMENTAL RESULTS

The overall performances of all the circuitry are comparatively shown as following in the table V.

Parameter	[16] 2019	[7] 2017	[15] 2017	This Work
V_{DD}	0.3 V	0.25 V	0.4 V	0.3 V
Technology	180 nm	130 nm	65 nm	54 nm
Type	ADSM	ADSM	DSM	ADSM
Power Consumption	37 nW	-	-	15.4 pW

Above are the comparison of results for different proposed works with some parameters. Present work was implemented in 54 nm CMOS technology with very low voltage and power.

Table.4. Transistor Aspect Ratios and Device Values

Device	W/L [µm/µm]
M_1, M_2, $M_{3A,B}$, $M_{4A,B}$, $M_{5A,B}$ - $M_{8A,B}$,	125/5
$M_{9A,B}$,M_{25A-C}	125/0.5
$M_{10A,B}$, $M_{11A,B}$, $M_{12A,B}$,	50/4
$M_{13A,B}$, M_{14}, $M_{17A,B}$, M_{24A-D},	60/1.5
$M_{15A,B}$, $M_{16A,B}$, $M_{18A,B}$-$M_{22A,B}$	25/0.5
$M_{23A,B}$	30/0.5
$M_{26A,B}$, $M_{27A,B}$	50/0.5
Device	value
C_1	50 pF
Inv1, Inv2 (p-MOS)	10/0.5
Inv1, Inv2 (n-MOS)	4/0.5

V. CONCLUSION

In this proposed work, we can achieve very low consumption of power which results in less consumption of area for hardware implementation with the very low voltage supply. Moreover, we can achieve larger size of data in output while increasing the number of bits used in digital to analog converter (DAC); but in this work implemented with only 1-bit DAC

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