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Low Power Dissipation and Low Power Consumption SRAM Architecture Based On 22-nm CNTFET Technology

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Abstract: -With the improvement of switching in Nano electronics, Carbon Nano Tube (CNT) could be explored in nanoscale Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Carbon Nanotube Field Effect Transistors (CNTFET) are encouraging nano-scaled devices for implementing high performance very dense and low power circuits. A Carbon Nanotube Field Effect Transistor belongs to the family of FET that utilizes a single CNT or an array of CNT's as the channel material instead of bulk silicon in the conventional MOSFET or Fin in FinFET structure. The fundamental of a CNTFET is a carbon nanotube. In this paper, the advantages of using CNTFETs are obtainable with respect to FinFET. The power dissipation, Power-delay product and power consumption of CNTFET's have been argued based on simulation through HSPICE Synopsys tool. This paper proposes a new design of low power SRAM cell using carbon nanotube FETs (CNTFETs) at 22nm technology node. CNFETs have received widespread attention as one of the promising successor to MOSFETs and FinFET. Analysis of the results shows that the proposed CNTFET based SRAM architecture, power dissipation, and power consumption substantially improved compared with the FinFET based SRAM cell by 97% and 97% respectively with almost same read delay.

Key Words— FinFET, CNTFET, Power dissipation, Power consumption, Static Random Access Memory (SRAM).

I. INTRODUCTION

For the foreseeable feature, static random access memory (SRAM) will likely remain as the embedded memory most important technology of choice for voluminous microprocessors and systems on chips (SoCs) due to the its speed advantage and compatibility with standard logic processes. With the beginning of SoC, the design of highly steady and power efficient SRAM structures has become highly very desirable. Therefore, it is important to improve a low power SRAM design method for the new device technology such as CNTFET. Carbon Nanotube Field Effect Transistor (CNFET) is the most promising technology to extend or complement the traditional silicon technology due to the following three reasons: First, the operation principle and the device structure are similar to FinFET devices, and the established FinFET design infrastructure can be utilized. Second, the FinFET fabrication practice can still be employed. And the most significant reason is that CNFET has the best experimentally proved device current carrying capability so far. A few looks into have been done to appraise the presentation of CNFET at a solitary gadget level in the participation of procedure related non-idealities and blemishes at the 22 nm innovation hub utilizing minimal CNFET SPICE model [3][4]. In this paper, as a circuit level design of CNTFET, a novel low power dissipation and low power consumption SRAM architecture design is proposed and its performance and viability are demonstrated by performing various simulations. The power dissipation and power consumption of SRAM architecture based on CNTFET are compared with that of the FinFET SRAM architecture design to show the viability of the CNTFET based SRAM architecture design.

The circuit simulation in this paper uses a 22nm CNTFET HSPICE model that includes the practical device non-idealities for CNTFET [6][7]. This paper has been systematized in the following manner: Section II explains the Review of CNTs and the characteristics and physical features of CNTFET Transistor are explained in Section III. Sections IV describe the mechanisms of the read and write operations of the proposed CNTFET SRAM architecture. The simulation results are presented in section V to compare the performance and viability of the CNTFET technology with that FinFET technology, and followed by the conclusion in Section VI.

II. REVIEW OF CNT'S

A Carbon Nanotube, discovered in 1991 by S. Iijima, is a sheet of hexagonal arranged carbon atoms rolled up in a tube of a few nanometers in diameter, which can be many microns long. Graphene is a solitary sheet of carbon particles arranged in the notable honeycomb structure [1] [2]. This lattice is shown in Fig. 1. Carbon has four valence electrons, three of which are used for the sp^2 bonds. In sp^2-hybridization an electron is promoted from the 2s-orbital to a p-orbital, and

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then two electrons from different 2p-orbitals combine with the single electron left in the 2s-orbital to generate three equivalent sp^2-orbitals.

These orbitals are planar with 120° between the significant lobess, and the rest of the p-orbital is perpendicular to this plane. The extra p-orbital is perpendicular to the graphene, and electrons in this orbital cling to other carbon molecules through feeble bonds. The electrons in the p-orbitals are along these lines inexactly headed and responsible for the conductance of graphite. Since the CNT is comprised of at least one sheets of graphene rolled up in a cylindrical structure, the binding in the CNT is about indistinguishable from that of graphite. The dissimilarities in bonding are because of the bigger between shell separation in CNT compared to the interlayer separation of graphite, and the twisting of the graphene sheets [8-10].

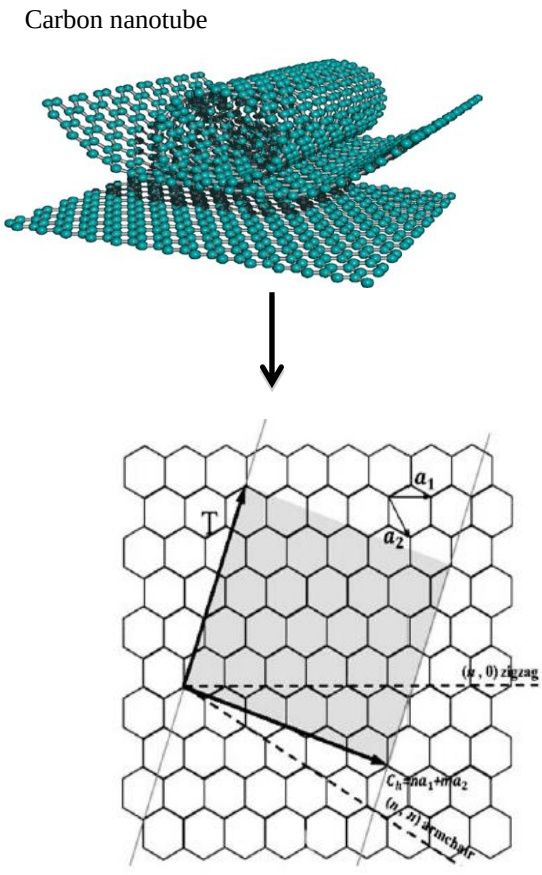

Fig.1. Lattice of graphene.

Fig.1. shows the structure of a graphene sheet, in which carbon atoms are positioned at each crossing and the lines specify the chemical bonds, which are resultant from sp^2-orbitals. C_h is chiral vector, T is tube axis; φ is chiral angle [1].

The chiral vector, C_h, is the vector which is perpendicular to tube axis T, which can be represented by:

$$C_h = n\,(\bar{a}1) + m\bar{a}2 \qquad (1)$$

Being n and m a pair of integers and a1 and a2 the lattice vectors, this can be written as:

$$\bar{a}1 = \left\{\sqrt{\tfrac{3}{2}}a_0, \quad \tfrac{3}{2}a_0, \right\} \bar{a}2 = \left\{-\sqrt{\tfrac{3}{2}}a_0, \quad \tfrac{3}{2}a_0, \right\} \qquad (2)$$

where, a_0 is the inter-atomic distance between each adjoining carbon atom and which is equal to 1.42 Å.

A CNT can be multi-wall (MWCNT) or single-wall (SWCNT) [1].

A MWCNT (Fig.2.) is made up of more than one cylinder whereas a SWCNT (Fig.3.) is a made up of single cylinder.

The CNTs shows either semi-conducting or metallic behavior depends upon the chiral vector. Especially, if n = m or n – m = 3i, where 'i' is an integer, the nanotube is metallic; otherwise, it shows semi-conducting property [1] [2].

The diameter of the CNT can be calculated by the following equation [1]:

$$d = \left|\frac{C_h}{\pi}\right| = \frac{a_0}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (3)$$

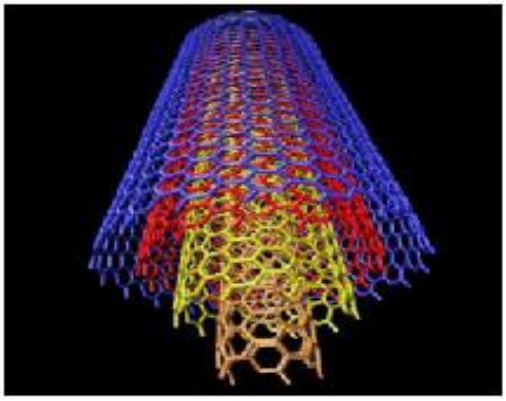

Fig.2. Structure of a MWCNT.

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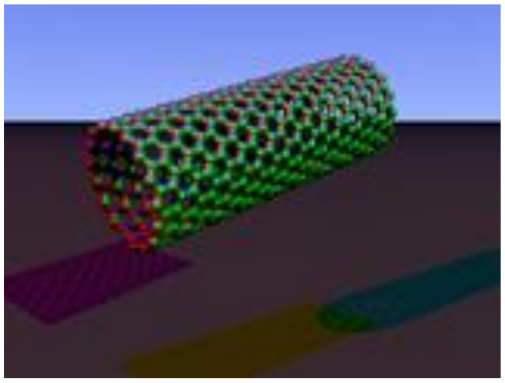


Fig.3. Structure of a SWCNT.

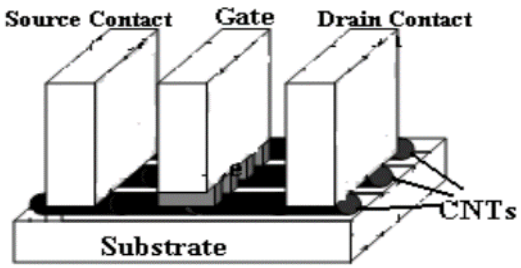
The chiral angle φ shows the chirality of nanotube and can be found by the following equation:

$$\cos\varphi = \frac{(n+m)\sqrt{3}}{2\sqrt{n^2+m^2+nm}} \quad (4)$$

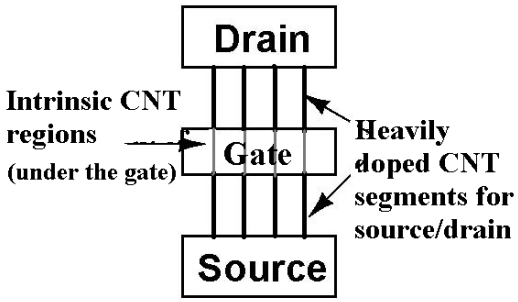
If (n = m, φ = 0°), CNTs are defined as armchair-type, while, if (m = 0, φ = 30°), as zig-zag type.

III. CNTFET TRANSISTOR

Carbon nanotube field-effect transistors (CNTFETs), as depicted in Fig.4., have been considered as a swap for, or supplement to, future semiconductor gadgets because of high portability, low imperfection structure, and inherent nanometre size of carbon nanotubes (CNTs). The incredible prevalence in execution for CNTFETs opposite best in class silicon gadgets has pulled in an extreme research exertion to investigate their application feasibility. Since the first CNTFET was created, CNTFETs have encountered extraordinary advances at the device structure just as gadget execution. CNT has two natures, metallic and semiconducting



(a)



(b)

Fig.4. Schematic diagram of a carbon nanotube transistor (CNTFET): (a) sectional view; (b) top view

The semiconducting property of CNT is utilized to produce CNTFET gadgets. Because of high conductivity property, SWCNT is by and large to a great extent utilized in CNTFET manufacture [11]

A. Types of CNTFETs

There are basically two types of CNTFETs on basis of device operation mechanism.

1. SBFET (schottky barrier FET)

2. MOS type FET.

Operation of CNTFETs

1-SBFET

The activity rule of carbon nanotube field-effect transistor (CNTFET) is like that of conventional silicon gadgets. This three (or four) terminal gadget comprises of a semiconducting nanotube, which acts as conducting path, spanning the source and channel contacts. The gadget is turned on or off electrostatically by means of the gate voltage. The semi 1D device structure provides channel length control by gate electrostatically than 3D devices (for example bulk CMOS) and 2D devices (fully depleted SOI) structures.

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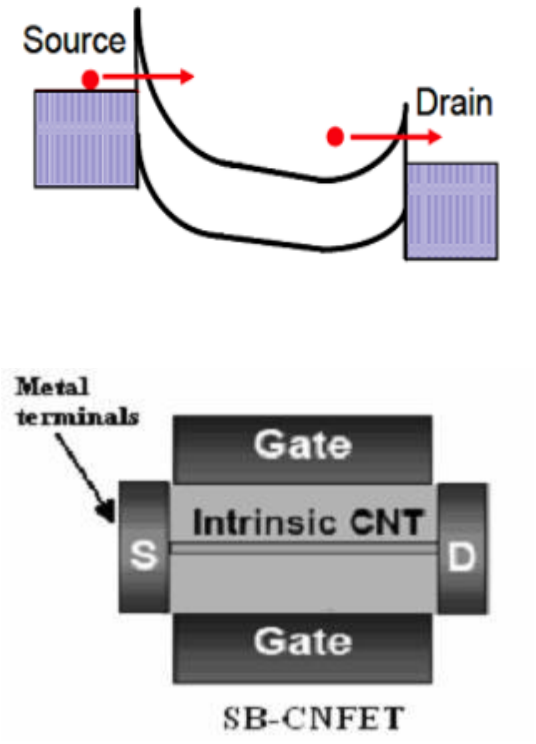

Fig.5. Schottky-Barrier CNFET (SB-CNFET)

The conductivity of SB-CNTFET represented by the majority carriers tunnelling through the SBs toward the end contact, the on-current and thus the device performance of SB-CNFET is dictated by the contact resistance because of the presence of tunnelling boundaries at both or one of the source and channel contacts, instead of the channel conductance, as shown in Fig.5.

The SBs at source/channel contacts are because of the Fermi-level arrangement at the metal-semiconductor interface. Both the height and the width of the SBs, and in this way the conductivity, are balanced by the gate electrostatically. SB-CNTFET shows ambipolar transport conduct. The work prompted boundaries toward the end contacts can be made to upgrade either electron or transportation of hole. In this way both the device polarity (n-type FET or p-type FET) and the device bias point can be balanced by picking the suitable work function of source/channel contacts.

B. 2-MOS type CNTFET

In MOS type CNTFETs cases, the drain and source are basically semiconductors, heavily doped with p-type or n-type. In the channel regions, the

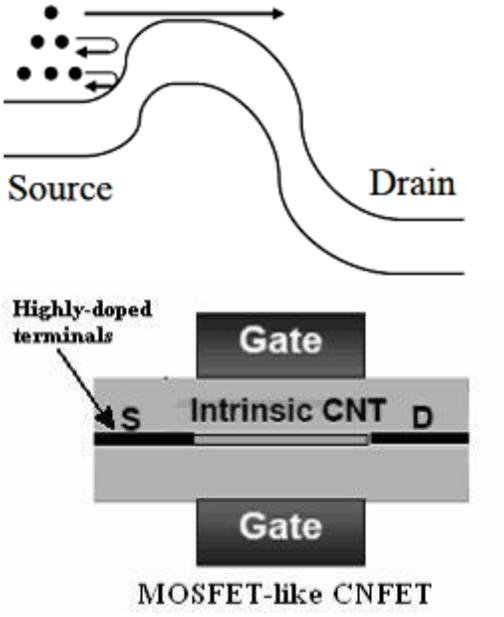

Fig.6. MOSFET-like CNFET

non-tunnelling potential barrier in the channel region, and in so doing the conductivity, is modulated by the gate-source bias voltage in similar way as in the silicon enhancement type MOSFET. The MOS type CNTFETs normally show a unipolar behaviour.

C. Characteristics of CNTFETS

The IV characteristics of CNTFETs can be understood to be similar as that of normal silicon MOSFETs. The current voltage curve can be divided into two regions: linear and saturation.

$$I_d = \frac{W}{L}\mu C_{ox}\left[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (5)$$

$$I_d = K_n[2(V_{gs} - V_T)V_{ds} - V_{ds}^2] \quad (6)$$

where K_n is conductance of CNTFET, W is the width of CNTFET, L is the length of CNTFET, μ is the mobility of carriers, C_{ox} oxide gate capacitance.

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Saturation current of CNTFET can also achieved by replacing $V_{ds(sat)} = V_{gs} - V_T$. Therefore, the saturation current of CNTFET can be expressed and written as:

$$I_{d\,(sat)} = K_n (V_{gs} - V_T)^2 \qquad (7)$$

IV. Proposed Differential SRAM Architecture

The differential SRAM architecture which has been proposed can store multiple bits in one complete block, as inside the case of a FinFET based SRAM. Fig.7. suggests proposed structure of the SRAM architecture which can stores i bits in a single block. The minimal operating voltage and region according to bit of the proposed SRAM rely upon the quantity of bits in a single block. A configuration that stores 3 bits in one block is chosen because the fundamental configuration via considering the stability between the minimum operating voltage and the area per bit. The proposed basic configuration SRAM architecture consists of 4 inverters which are in cross-coupled pairs, block mask transistors (MASK-1 and MASK-2), write access transistors (WR-1 and WR-2), pass gate transistors (PGL1~4 and PGR1~4), read buffers (RD1 and RD2), cross-coupled pMOSs (P2 and P3), and a head transfer switch (P1). The read WL (RWLB), the block selects signal (BLK), and WLs (WL1~4) are row-based signals, while write BLs (WBL and WBLB), the write WL (WWL), and read BLs (RBL and RBLB) are signals which are column-based. During the hold state, WLs, WWL, and WBLs are held at zero V. BLK is held at V_{DD} to connect the WBLs and the LBLs, so that the LBLs are discharged to zero V and the read buffers are becoming OFF.

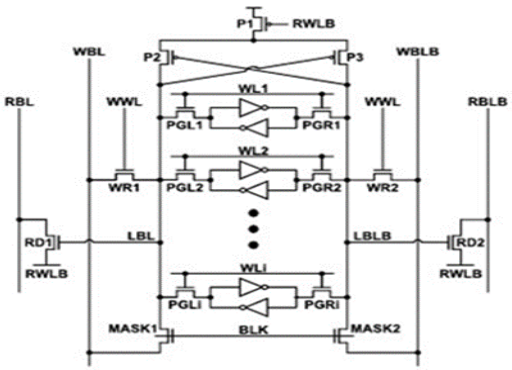

Fig.7. Proposed SRAM architecture that stores *i* bits in one block.

Further, the RWLB is likewise held at V_{DD} to turn OFF the head transfer switch and to stop the RBL leakage current.

A. *Read Operation*

The read operation of the proposed SRAM architecture is defined in Fig.8(a). This operation is carried out in phases. During the first Phase, BLK of the chosen block is forced to stay at 0 V, and the chosen WL is enabled. On the basis of the saved information, even though the voltage of the LBL that is linked to the 1 Storage node will become high, its value can't be as high as that of the entire V_{DD} due to the V_{th} drop via the skip gate transistor, and the voltage of the opposite LBL remains low. During read operation, as RWLB is high within the first phase the RBL is not discharged. With the assertion of WL, although the 1 storage node is disturbed, the read disturbance is small due to the small capacitance at the LBL. This smaller read disturbance makes the proposed SRAM be capable of perform in extensively decreased running voltage. The Second phase starts off evolved with the falling of the RWLB. As soon RWLB is asserted, it enables not only the discharge of the RBL however additionally the feedback of cross-coupled pMOSs.

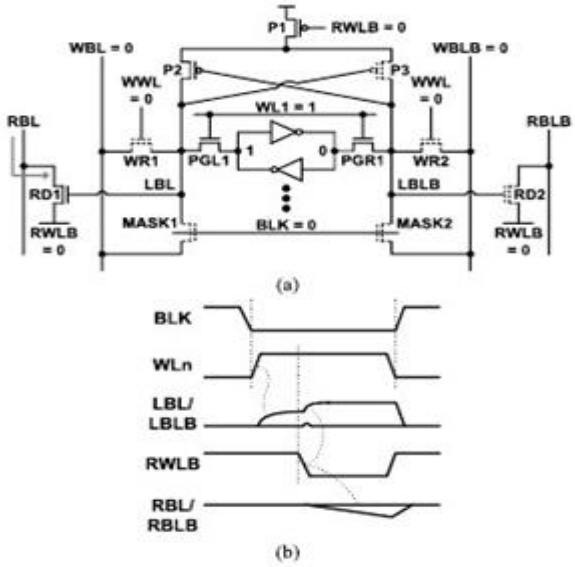

Fig.8. (a) Read operation and (b) read Operational waveform of proposed SRAM architecture.

Positive feedback of the cross-coupled pMOSs increases the LBL to the value of the full V_{DD}, due to which the LBL can acquire a full swing, and the gate of the read buffer is driven by means of the full V_{DD}, without the need for a boosted WL voltage. Thus, under scope of the proposed SRAM architecture which is totally based on an very advanced technology, read stability can be enhanced with the

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suppressed WL voltage, without degradation of the read delay. In different words, the gain of the proposed SRAM architecture is that it eliminates the trade-off among the read stability and the read delay. The read stability can be enhanced by suppressed WL voltage, and also, the read delay can be minimized by the full-swing LBL. In the SRAM architecture, proposed in this paper, read current has been increased via a single nMOS used as the read buffer, and RBL leakage current is reduced by the use of attached buffer foot. The read buffers are turned OFF when the column half-selected block is in the hold state, so that the RBL leakage is not disturbed with the column half-selected block.

In the SRAM structure proposed, it is very important to manipulate carefully the sign timing to keep away from the data from flipping, as shown in Fig.8(b). The WBL and the 1 storage node when held at 0 V will be connected as both the BLK and the WL are high simultaneously, causing the data to flip. Thus, after the fall of BLK is completed then only the WL should be asserted. Despite the variations in Vth, sufficient LBL development is required for the robustness of the good feedback of the cross-coupled pMOSs. Thus, the assertion of RWLB should be done with a sufficiently large timing margin, after the WL is asserted; this requires a further timing overhead. A critical factor to be aware right here is that the total read delay of the proposed SRAM primarily based on an advanced technology together with the 22-nm FinFET era is slightly more but almost same as compared to CNTFET SRAM architecture.

B. *Write Operation*

The write operation of the proposed SRAM

architecture is shown in Fig.9(a). As shown in figure, BLK of the block selected is forced to linger at 0 V, and the chosen WL is enabled. Further, the WWL is compelled to stay at V_{DD} so that the write access transistors are grew to become ON, and the WBLs are pressured to remain at a positive voltage level on the basis of the write information. The WBLs are linked to both the storage nodes through write access transistors and pass gate transistors because of which the write operation can be said to be differential, and in the proposed SRAM architecture, the write ability is achieved.

The row half-selected block shown in Figure 9(b) is within the identical circumstance as during the read operation, except that the RWLB is high. Although the storage nodes of the row half-selected blocks are disturbed throughout the write operation, the disturbance is small due to the small capacitance at the LBL. Thus, need for the write-back scheme is eliminated and the steadiness of the row half-selected block is ensured.

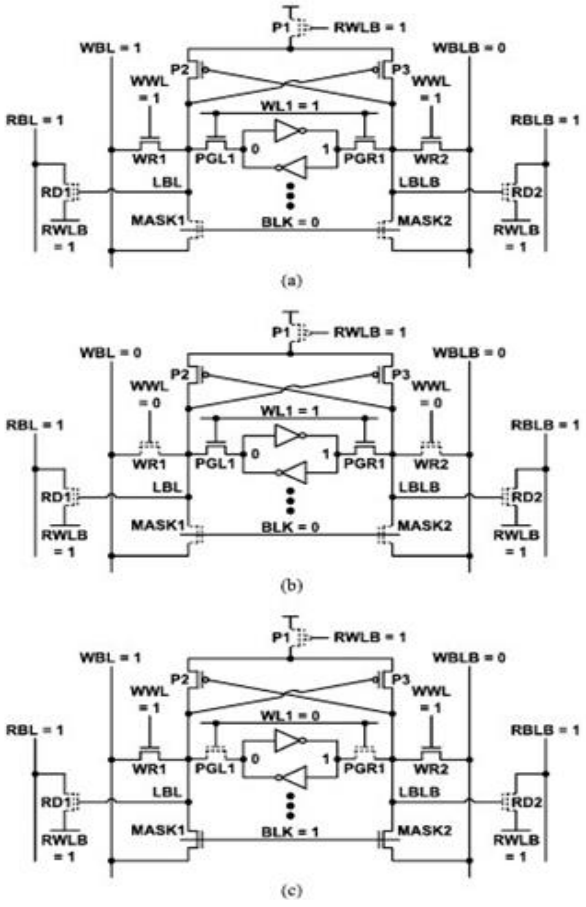

Fig.9. (a) Selected, (b) row half-selected, and (c) column half-selected blocks of proposed SRAM architecture during write operation.

Further, it can be summarised unnecessary RBL leakage has been eliminated by using a buffer foot which resulted in saving large amount of dynamic power in the proposed SRAM architecture. Also, the static power consumption has been reduced largely due to the dc current path in the column half-selected block being eliminated by connecting the sources of the block mask transistors to the WBLs.

Hence, heat dissipation and its effect on current in carbon nanotube (CNT) MOS like CNFET due to the tube channel is smaller than Fin channel used in FinFET.

C. *Layout*

Fig. 10 suggests the layout of the basic configuration of the proposed SRAM structure based totally at the 22-nm FinFET era, designed with the smallest transistors. The local interconnect within the middle of line is employed to reduce the number of metallic layers [12]. V_{DD} and V_{SS} are routed in

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metal 1; the LBLs are routed in metallic 2; the BLK and RWLB are routed in metal 3; the RBLs, WBLs, and WWL are routed in metal 4; and the WLs are routed in metal 5.

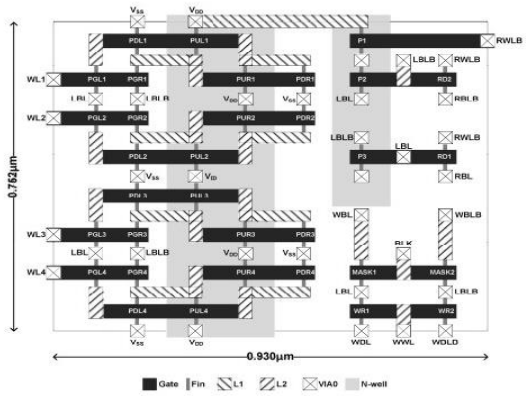

Fig.10. Layout of the proposed SRAM architecture based on the 22-nm CNTFET technology.

V. Simulation Results And Comparison

The structure of the proposed SRAM is demonstrated via the HSPICE Synopsys simulation tool. In Figure 11, a bar chart is presented, which clearly states that by the use CNTFET over FinFET, a large amount of Average Power is reduced. Fig.12. show a bar chart which shows that the power dissipation has also been greatly reduced by using CNTFET in place of FinFET based SRAM architecture. The bar chart shown in Fig.13. depicts delay in the techniques. As the path of signals is same, the Delay in FinFET and CNTFET technique is almost same. Due to the increased demand for high-speed, high-throughput computation, and complex functionality in mobile.

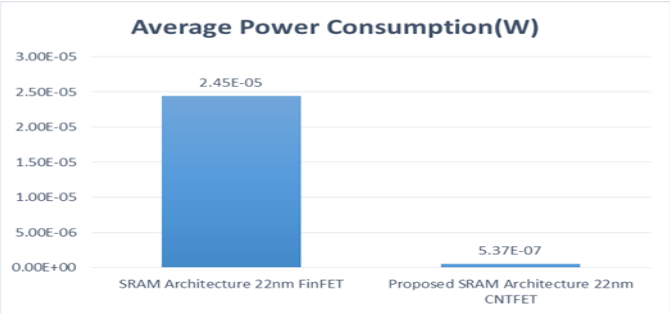

Fig.11. Comparison of average power of 22nm FinFET SRAM architecture with 22nm CNTFET SRAM architecture

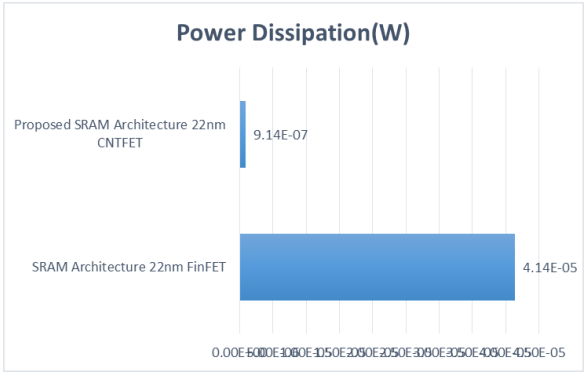

Fig.12. Comparison of power dissipation of 22nm FinFET SRAM architecture with 22nm CNTFET SRAM architecture.

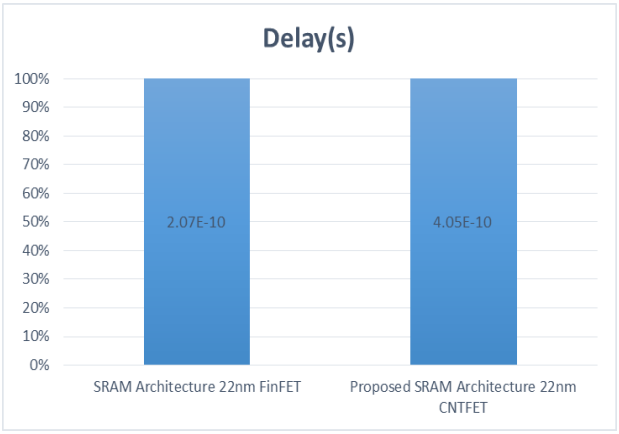

Fig.13. Comparison of delay of 22nm FinFET SRAM architecture with 22nm CNTFET SRAM architecture.

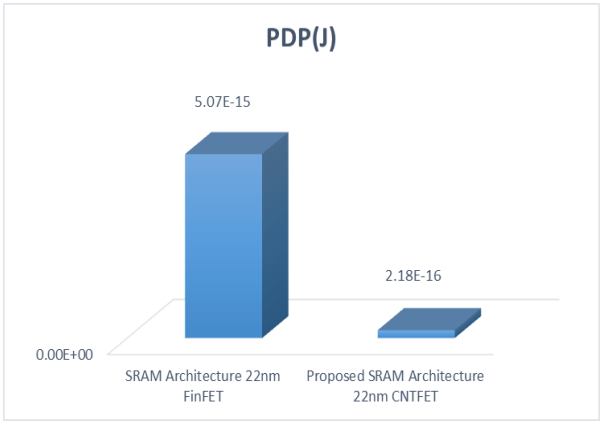

Fig.14. Comparison of power delay product (PDP) of 22nm FinFET SRAM architecture with 22nm CNTFET SRAM architecture.

environments, reduction of delay and power consumption is very challenging. FinFET and CNFET can be compared using the Power Delay Product (PDP) as metric. Table 1 shows the delay, average power consumption, and Power Delay Product (PDP) of logic gates in 22nm FinFET and 22nm CNFET technologies; the PDP of the 22nm FinFET is about 95 times higher than that of the 22nm CNFET.

Table.1. Overview of simulation results

Description	SRAM Architecture 22nm FinFET	Proposed SRAM Architecture 22nm CNTFET
Average Power Consumption(W)	2.45E-05	5.37E-07
Delay(s)	2.07E-10	4.05E-10
PDP(J)	5.07E-15	2.18E-16
Power Dissipation(W)	4.14E-05	9.14E-07

VI. Conclusion

This paper has investigated the use of MOSFET-like CNTFET in place of the FinFET while designing the SRAM architecture. This new CNTFET SRAM architecture is compared with FinfET based SRAM architecture. In the SRAM architecture proposed Full-Swing Local Bitline is achieved without trade-off between read stability and read delay. A Full-Swing Local Bit Line is achieved using cross-coupled pMOSs and accordingly read buffer contributes towards enhancing the read delay. Further, the uncoupled nMOS read buffer contributes towards enhancing the read delay. In addition, the useless RBL leakage for the duration of the write operation is removed via the usage of the read buffer with a buffer foot, ensuing within the saving of power throughout the write operation. Compared to FinFET structure, the proposed CNTFET SRAM saves power consumption up to 97% and power dissipation upto 97% with minimal cost of 0.02% delay increase. Post simulation results ithas been observed that the CNTFET based SRAM architecture design achieves improvements in power consumption, especially at a low power supply.

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