An Investigation of Comparators in Flash ADC

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Abstract: - Analog-to-digital converters (ADCs) are devices that allow computers to communicate with analog signals, which are typically used in manufacturing processes. ADC technology has become increasingly important in recent years as computers become more commonplace in factories and other industrial settings. Semiconductor manufacturing is important for modern technology, and a key part of this process is using semiconductor wafers. These wafers are thin sheets of metal that are used to create electronic devices. An ADC is a device that can convert an analog signal into a digital one, which can be processed more quickly and easily. This is important because it allows for more accurate and faster measurements. One type of ADC, known as a flash ADC, is especially fast and can support high-bandwidth applications, such as optical communications and radar detection. Flash ADCs are especially helpful for tasks like optical communications and radar detection, which require high speeds and high bandwidth. The comparator circuit is responsible for comparing the input signal to a set threshold value and determining the appropriate conversion result. This circuit can affect the overall performance of the ADC, so it's important to choose the right one for your application. There are many different comparator architectures, and some are more efficient than others. Some architectures are more effective at comparing two values than others. In this paper, we compare different comparator designs to find the best one for future flash ADC designs. The high-performance comparator we find is very efficient and should be used in future flash ADC designs.

Key words: ***comparator, flash, ADC, VLSI, memory.***

I. Introduction

Signals produced by nature are analog, usually representing varying quantities in continuous time. However, given the processing and storage advantages of digital signals, ADCs are designed to convert continuous-time analog signals into discrete-time binary-code digital signals. Low-power, high-speed ADCs are in high demand in many applications, such as in medical imaging applications such as magnetic resonance imaging (MRI) and computed tomography (CT) [1]. For wearable biomedical applications, it is important to conserve power [2]. There are different ADC architectures with their own advantages and drawbacks. Flash ADCs are the fastest option because of their parallel structure. [3], However, their higher footprint and power consumption cost mean they have a lower performance than many competing products. This document consists of three parts. First, Section 2 briefly describes the flash ADC architecture. Second, Section 3 compares various comparator topologies. Third, Section 4 concludes with a recommended topology

Manuscript revised April 03, 2023; accepted April 04, 2023. Date of publication April 07, 2023.

This paper available online at www.ijprse.com

ISSN (Online): 2582-7898; SJIF: 5.59

II. Material and Experimental Methods

Figure 1 shows the general structure of a flash ADC. This ADC consists of a resistor, a comparator, and an encoder circuit. A scaling resistor is used to provide a series reference voltage. One end of the series resistors is connected to the diode flash ADC and the other end is connected to the diode flash ADC. At least two resistors are required to divide the reference voltage by the reference voltage 2^n-1. The comparator is the most important component that determines the overall performance of a flash ADC. Building a single-bit ADC requires the use of at least 2^n-1 comparators. Each of the relevant reference voltages of the resistance scale is connected to a comparator, and the +s of all comparators are connected to the input voltage. The comparison of the input voltage to the reference voltage is a boolean 1 or 0. The encoder directly converts the thermometer code generated by the previous comparison to a binary code.

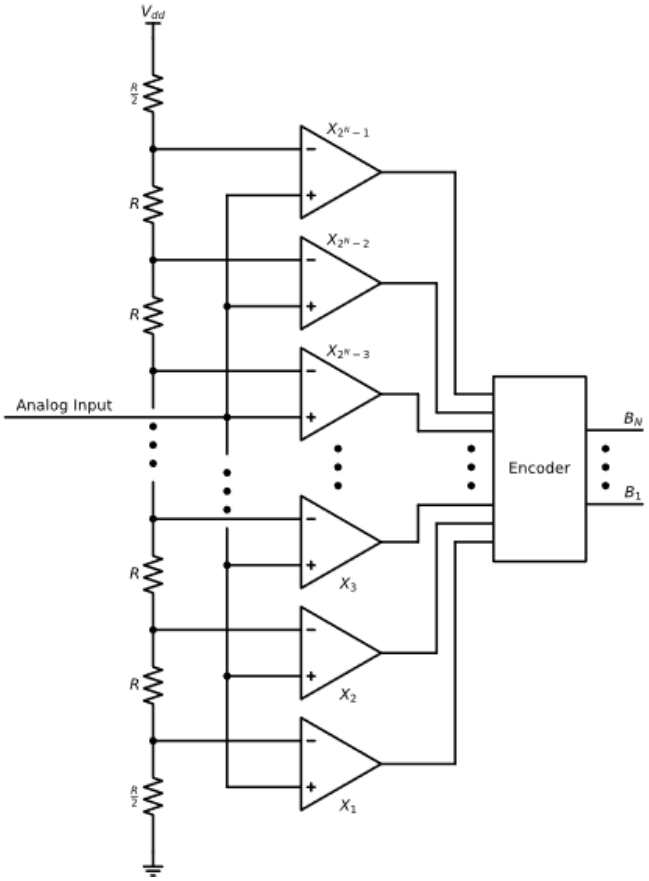

Fig.1. Fully Differential Two-Tail Comparator Schematic

III. MATHEMATICAL MODEL

To find the best high-performance flash ADC, the authors compare different comparators for power consumption and latency.

3.1 Traditional Comparator

A typical comparator usually consists of two stages: a preamplifier stage and a latch stage. The two-tier structure is shown in FIG. In the reset phase, M4 and M5 are both on to discharge the first stage output and M1 is off to prevent the output from being charged. M6 and M9 are included to charge the output of later stages to VDD. In the evaluation phase, CLK is high and clk is low. Then the results of the first step begin to change. The rate of charge depends on the ratio of the current flowing through the transistor to the node capacitance. Gradually, the first stage creates a differential voltage at the output node due to different charging rates. The dynamic latch is activated as soon as the output voltage exceeds the trigger voltages M10 or M11. The positive feedback function of the latch causes one of the node's output voltages to reach VDD and short the other to GND. Both outputs of the preamplifier stage eventually reach VDD. In this topology, the first stage output is charged during the evaluate phase and discharged during the reset phase, requiring large transistors and incurring significant power dissipation. These disadvantages make these conventional comparators unsuitable for low-power applications. Figure 2 shows.

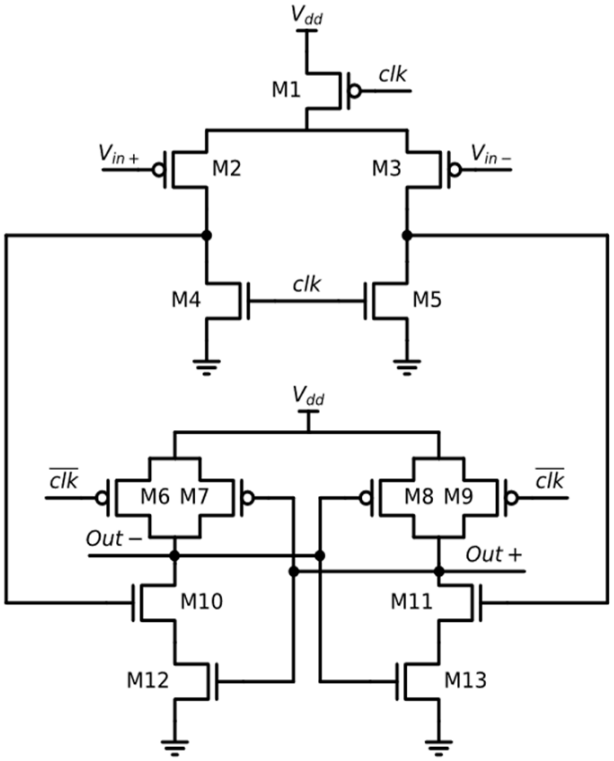

Fig.2. Schematic diagram of traditional comparisons

3.2 Comparator With Improved Trans Conductance

This comparator has a slope increased to reduce latency. When $clk = 0$, we charge the output of the previous phase to Vdd. M6, M7 on, M8 and M9 off. The stage's output is charged to VDD through M6 and M7. Early in the evaluation phase, clk' is delayed so that M8, M9 can be turned on later to reduce short current power consumption through M10 and M13. The final output node is discharged from VDD and D+ and D- are charged from GND. Transistors M6, M7, M11 and M12 therefore operate in triode mode. When clk' = 1, since M8 and M9 are on, the output of stage 2 is quickly discharged to D+/-. The final output is then clamped to VDD or GND. The overall tilt of this latch design is higher and faster than its counterparts.

These benefits allow these comparators to perform comparisons faster and consume less power. Figure 3 shows.

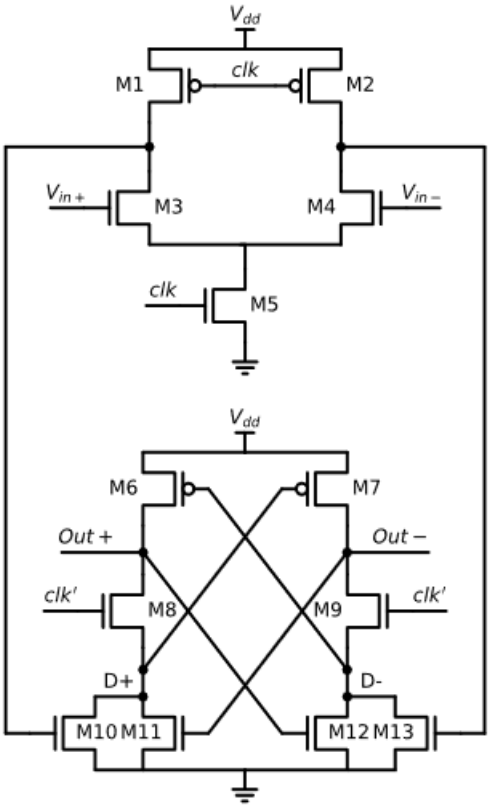

Fig.3. Schematic diagram of a comparator with enhanced conductivity.

IV. A Comparator with Two Stages of Comparison Is Known as An "Improved Two-Stage Comparator

This figure 4 shows an upgraded two-stage comparator. CLK, CLK', and CLK' go high at the reset stage, unloading the preamplifier output and latching it to GND using M14 and M17. In the evaluation stage, CLK and CLK' initiate the preamplifier by switching to 0. Using the crossover circuit M4 and M6, differential voltage is boosted while common-mode voltage is lowered in the first stage output, providing a strong driver for the latch stage. Finally, clk' is set to 0 to activate the PMOS latch, and meanwhile, clk' is toggled to 1 to disable M1 and reduce power consumption. This comparator design has two features: a cross-coupling circuit for higher preamplifier gain, and a series lock to reduce power consumption and turn the preamplifier on/off.

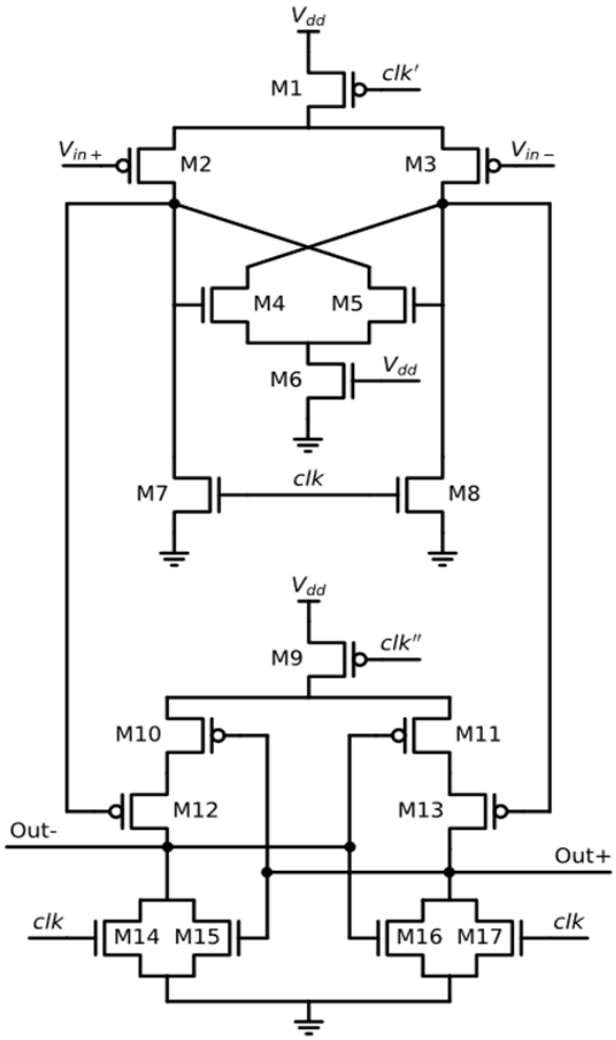

Fig.4. The comparison block scheme has been improved in two stages.

V. Fully Double Differential Comparator

The Figure 5 differential comparator has illustrated reset and evaluation modes. In reset mode, transistors M1, M2, M8, and M11 are closed. The output of the first and last stages is replaced by VDD. When CLK goes high, the comparator is in evaluation mode. Transistors M1, M2, M8, and M11 are open to stop charging. The output node of the second stage is discharged to GND via transistors M3-6 and carefully adjusted to provide equal currents. In evaluation mode, the final output is either closed to VDD or GND depending on the difference in input voltage between the first and second stages. This comparator design uses transistors M1 and M2 to convert a single-ended comparator into a two-ended comparator with

differential inputs to reduce power loss and provide voltage compensation with an acceptable propagation delay.

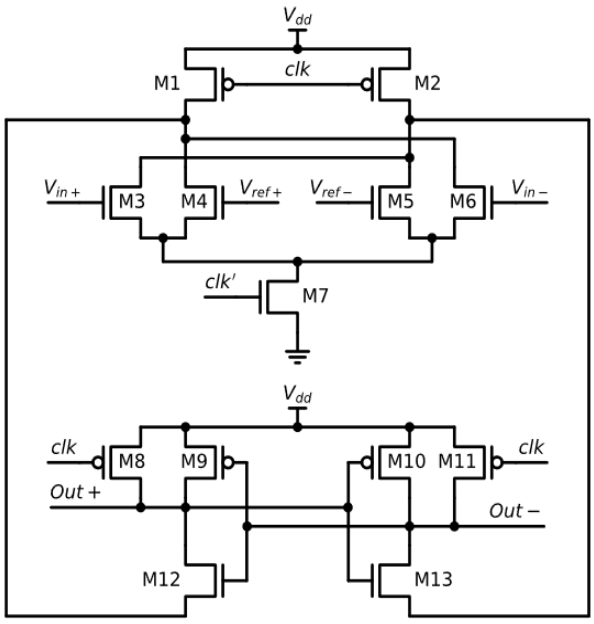

Fig.5. Dual Tail Diff. Comp. Circuit

VI. Comparison Decision

Different comparator designs use different methods to reduce power consumption, delay, and increase operating frequency. The improved trans conductance comparator has the highest power consumption, and the improved two-stage comparator has the lowest propagation delay on Figure 6.

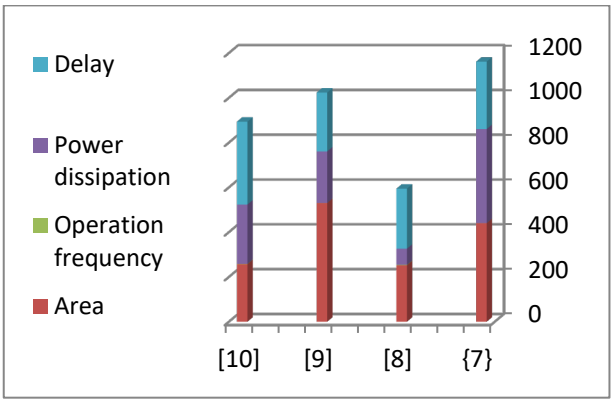

Fig.6. There are several different comparator topologies, each with its own advantages and disadvantages.

VII. Conclusion

This paper compares several new comparator topologies for flash ADCs. Of the comparators mentioned, the enhanced conductivity comparator has the lowest power consumption at 72.2 watts and can operate up to 2 GHz. Therefore, building a flash ADC using this comparator structure is a relatively suitable choice for low-power, high-speed applications. Future work will include implementing a flash ADC using the comparator structure described above and measuring the propagation and overall delay of the ADC.. Reducing the number of comparisons made in the flash ADC can help improve performance. This can be done by using a buffered data structure, which can reduce the number of reads that need to be performed.

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