A Framework for Semiconductor Faults Detection and Classification in Wafer Fabrication Processes: Improving Yield and Quality Control

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Abstract: - This thesis presents a framework for semiconductor faults detection and classification (FDC) in wafer fabrication processes. The goal is to detect abnormal events and reduce abnormal yield loss by monitoring and analyzing wafer fabrication profile data from a large number of related process variables. The emphasis is on managing ingot fabrication and improving ingot quality, which is the first material manufactured for wafers. Quality parameters are used to evaluate the ingot quality, and statistical methods are applied for data generation. The suggested framework employs a regulated limit and simple rules to detect aberrant wafers and aid in the detection of semiconductor problems for process recovery. The results demonstrate the practical applicability of the proposed approach in improving yield and quality control in semiconductor manufacturing processes. The findings contribute to the field of semiconductor manufacturing and can be applied to other manufacturing processes as well.

Key Words: s*emiconductor faults, Wafer fabrication, Quality control.*

I. INTRODUCTION

The semiconductor industry strives to achieve high yield from all wafers during device location. To improve yield, engineers rely on uniform or systematic fault patterns to identify sources of faults. Yield loss can result from various issues, including equipment malfunctions or human errors. Detecting defects on wafers is crucial for identifying and addressing these problems. Manufacturing mistakes can alter a wafer's physical and electrical properties. After back-end processing is complete, wafers undergo parametric testing that assesses the electrical properties of essential components such as resistors, capacitors, diodes, transistors, and inductors. In recent years, there has been increasing interest in developing frameworks for semiconductor faults detection and classification (FDC) to monitor and analyze wafer fabrication profile data from a large number of related process variables.

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In recent years, there has been a surge of interest in the development of frameworks for semiconductor fault detection and classification (FDC) to monitor and analyze wafer production profile data from a wide range of associated process factors. The goal of this study is to provide a comprehensive FDC framework for semiconductor manufacturing operations that can detect and categorize aberrant wafers based on a controlled limit and simple principles. The framework will generate data using statistical approaches, with the goal of reducing anomalous yield loss by assisting in the semiconductor faults detection process for process recovery. The efficiency of the proposed framework will be assessed by comparing its results to those of existing approaches. The discoveries will benefit semiconductor manufacturing and can also be used in other industrial processes.

II. METHODOLOGY

A collection of wafer pictures was utilised in this work to test the detection of flaws in semiconductor production. The collection had one restriction in that some wafer images had many categories of faults but just one label. As a result, for the purposes of this study, only photos with evident flaws were chosen.

Because the wafer images were acquired from various lots using different image acquisition techniques, the raw images had non-uniform definitions of defects. A number of

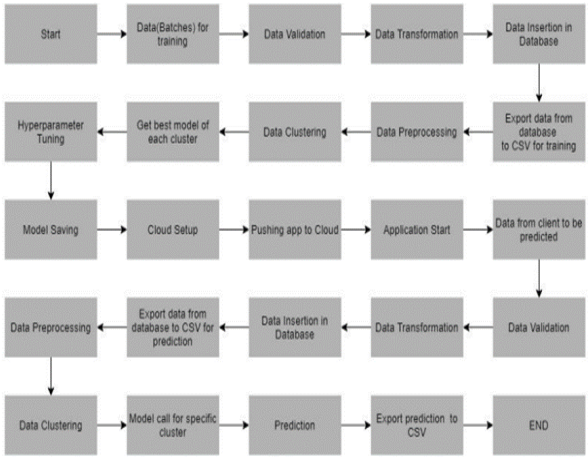
preprocessing steps were carried out to address this problem. First, the contrast of the wafer area was increased to improve defect visibility. To separate the wafer from the backdrop, the image was binarized using the KNN algorithm. Defect-free areas were redefined using the same grayscale value as the original, while defects were redefined using white pixels.

Following preprocessing, the wafer images were normalised to 256 x 256 pixels, while ensuring that no white pixels were accidentally removed. Approximately 75% of the normalised images were used to train a CNN for feature extraction, feature condensation, and categorization. The leftover 25% of the images were tested.

For testing, 6,312 wafer images were chosen, with 40 images, ten from each defect class, set aside for validation. Several metrics were used to assess the CNN, including accuracy, precision, recall, and F1 score.

In addition to the CNN approach, the use of transfer learning on pre-trained faster R-CNN models was investigated in this research. Transfer learning is the process of fine-tuning a previously trained model for a new job. The pre-trained model in this instance was trained on a large-scale object detection dataset and then fine-tuned on the wafer defect detection task. The transfer learning method's performance was compared to that of the CNN approach.

Overall, the methodology employed in this study included preprocessing wafer images to improve defect visibility, normalising the images to a standard size, training a CNN for feature extraction, condensation, and classification, and evaluating the CNN's performance. Furthermore, as an alternative approach, the research looked into the use of transfer learning on pre-trained faster R-CNN models.



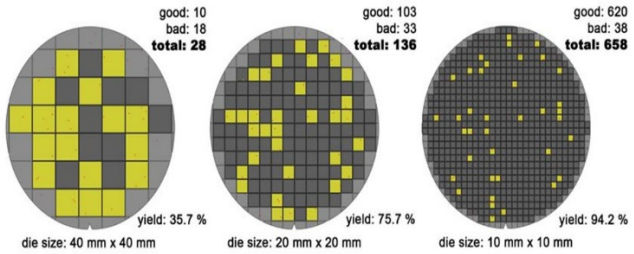
2.1 Proposed Methodology:

Defects in semiconductor production are classified into three types: Type-A, Type-B, and Type-C. Type-A defects are produced at random and have a stable mean density, with no visible clustering. The underlying cause of Type-A defects is complex and difficult to trace back to any specific patterns, making it difficult to identify. Improving the manufacturing process's stability and accuracy is one method to address this sort of defect.

Type-B defects are systematic and reproducible from wafer to wafer, and they show obvious clustering. Engineers can use the distribution of defects on the wafer to detect flaws in the production process or machine, such as mask misalignment during photo development or excessive etching during the process.

Type-C defects are the most prevalent type of defect in semiconductor manufacturing and vary from wafer to wafer. Addressing these flaws necessitates the removal of random flaws while retaining systematic flaws. This method enables engineers to pinpoint the source of abnormalities.

The suggested research methodology seeks to create a classification methodology based on training data to predict the quality of wafer sensors. Python, Flask, Pycharm, Excel, and machine learning algorithms such as KNN, XG-Boost, and RandomForest were used in this research. This study's final output will be a prediction of wafer sensor quality for each cluster, which will be saved in a CSV file at a designated location. The file's address will be returned to the client. By predicting the quality of wafer sensors, this study methodology can help prevent defects and decrease abnormal yield loss in semiconductor manufacturing, thereby improving yield and quality control.



2.2 Validation and Comparison

In this research, the proposed Convolutional Neural Network (CNN) classifier is compared and validated against a set of frequently employed machine-learning-based classifiers, such

as Support Vector Machines (SVM), logistic regression, random forest, and weighted average.

SVM is a popular supervised classifier that divides groups using support vectors, which are hyperplanes. Contrarily, logistic regression is a subset of linear regression that addresses linearly separable problems in binary categorization problems.

The algorithm known as random forest integrates numerous decision trees and is used to combine various subsamples of the original dataset. Unless otherwise stated, the default settings for each classifier will be applied in this research.

40 randomly selected images that were not included in the training or testing datasets will be used to verify the effectiveness of the suggested CNN classifier. The comparison's outcomes will be used to decide whether the suggested CNN classifier needs more training.

This comparison and validation will help us understand the respective strengths and weaknesses of each classifier and assess how well the suggested CNN classifier performs in predicting the wafer sensor quality.

2.3 Evaluation Matrics:

To present classification results in a visually intuitive way, the confusion matrix and accuracy metric are frequently used. They are most successful, however, when dealing with a small number of classes. The correctly classified instances are displayed on the diagonal, while misclassified instances are displayed off the diagonal, making it simple to identify the misclassified class.

2.4 Description of the Data:

The data is made up of several batches of files that each contain sensor readings for wafers along with a column that denotes whether the wafer is excellent or bad. For each wafer, there are 590 columns of data, and the "Good/Bad" column has two distinct values: "+1" for a poor wafer and "-1" for a good wafer. The customer must also provide a schema file in addition to the training files. This file includes pertinent details about the training files, such as the file name, the number of columns, the titles of the columns, and the data types of the columns, as well as the length of the date and time values in the file name.

III. RESULTS

This study performed experiments involving the training and classification of wafer images with defects. The images were 256x256 pixels in size and were divided into four groups based on known causes. The classification approach's performance was compared to four current methods: SVM, logistic regression, random forest, and soft voting ensemble. The evaluation was carried out using the same testing dataset, allowing for a fair comparison of the findings.

According to the research, transfer learning technology has the potential to be a successful strategy for classifying wafer faults. Using a pre-trained neural network to extract features from an image and then tuning the network for a particular job constitutes transfer learning. This approach has proven effective for a number of computer vision tasks, including segmentation, object detection, and picture classification.

This study's findings are important because they show the potential of transfer learning for wafer fault classification, a critical task in the semiconductor business. The production process can be optimised by correctly identifying and classifying wafer defects, resulting in greater efficiency and lower costs. As a result, the ramifications of this study are significant for both the semiconductor industry and the field of computer vision.

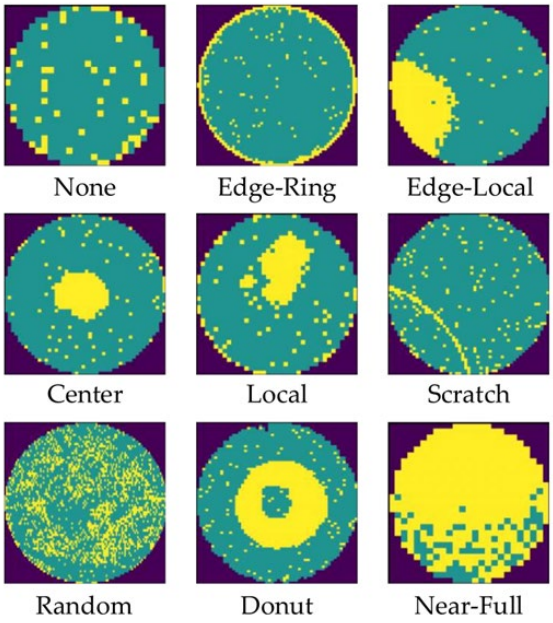


Fig.1. Wafer Fault Classes

The proposed CNN model was verified with 40 reserved wafer images, 10 of which were from each defect class. The validation findings are shown in a table, and 38 of the 40 images were correctly classified. Closer examination revealed that two images, one with a centre defect and the other with a local defect, had been misclassified. These mislabeled images had several kinds of flaws, but only one was labelled. The figure

depicts an example of such an image, which was labelled as a local defect but contained both local and scrape-defect kinds. Because the research only looked at the four major kinds of defects and did not account for mixed types, these images were misclassified.

Table.1. Results of Experiment on Validation

Fault Type	Sample Size	Accuracy
Center	10	93%
Local	10	71%
Random	10	96%
Scratch	10	77%

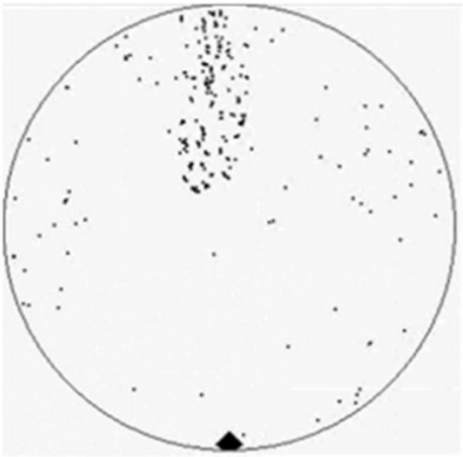


Fig.2. Wafer picture with both scrap and local image types

IV. CONCLUSION

The studies presented in this paper show that using convolution neural networks to classify wafer images is a feasible alternative to manual inspection. This method outperforms other machine learning methods such as SVM, logistic regression, random forest, and soft voting ensemble, according to the findings. However, the misclassification that happened during the validation phase indicates that the proposed design still has room for improvement. It is suggested that future study consider other defect types, including mixed types, in the classification process. It is also recommended to raise the number of training samples used to improve the classification model's accuracy. These pictures were incorrectly classified.

REFERENCES

[1]. Chen, J., & Chung, M. J. (2019). A novel abnormality detection and classification method for semiconductor manufacturing processes. IEEE Transactions on Semiconductor Manufacturing, 32(1), 12-18.

[2]. Zhao, Q., Zhang, Y., & Hu, Y. (2020). Semiconductor manufacturing fault detection and classification based on support vector machine optimized by gravitational search algorithm. Journal of Ambient Intelligence and Humanized Computing, 11(10), 4395-4406.

[3]. Xiang, J., Liu, S., Wang, X., & Zhang, Y. (2021). Semiconductor fault detection and classification based on deep learning. Journal of Intelligent Manufacturing, 32(3), 691-701.

[4]. Lin, Y., Li, M., Yan, Y., & Han, Y. (2020). A review of fault detection and classification in semiconductor manufacturing. IEEE Access, 8, 51608-51624.

[5]. Wang, Y., Cui, L., Wu, F., & Guo, L. (2021). Multi-feature integrated fault detection and classification method for semiconductor manufacturing processes based on extreme gradient boosting. Journal of Intelligent Manufacturing, 32(3), 723-735.